REMARKS

Claims 1, 3-6, 8-10, 12-15, and 17-27 remain in the application and have not been further amended.

Reconsideration is respectfully requested of the rejection of the claims under 35 U.S.C. 103(a), as being unpatentable over *Smolansky, et al.* in view of *Takai*.

Exemplary embodiments of the present invention are intended to permit the data width of an input/output buffer to be changed contemporaneously with memory access operations. A row address relating to the buffer is provided to a decoder along with read and write control signals. The decoder produces a width control signal that is fed to an input buffer controller and an output buffer controller. Depending upon the status of the read/write signals, the input control signal is generated or the output buffer control signal is generated. These control signals control the input/output width of the input buffer and the output buffer.

The decoder is shown in FIG. 7 and includes switches that receive the address signals, as well as a logic circuit that receives the read and write signals. The output of the switches form the control signals that control the width of the buffer.

The above-noted features of the present invention are set forth in the independent claims as currently amended.

Smolansky, et al. discloses an adjustable width FIFO buffer for variable width data transfers. In FIG. 3 thereof, an address decoder 102 is employed and as stated in column 7 of *Smolansky, et al.*, the address decoder 102 provides a decoded address to register read control logic 90. The register read control logic selects one of the odd registers to which the data is to be written to. Alternatively, one of the even registers may be selected. Nevertheless, it is respectfully submitted that the decoder of *Smolansky, et al.* does not provide the width control signal as in the presently claimed invention.

Therefore, it is respectfully submitted that the data buffer controller of *Smolansky, et al.* is not the same as the buffer controller of the presently claimed invention.

Takai is cited for allegedly showing the details of the decoder as recited in the present claims. Although *Takai* does show column address decoder/selector units in FIG. 5, for example, these units provide only a bit, that is, a read-out or write-in data bit. There is no suggestion that this information is utilized as a width control signal fed to the data buffer controller, as in the presently claimed invention.

It is clear that the data width control circuit of the presently claimed invention is different and distinct from the column address decoder units of *Takai*.

As described in *Takai* at column 10, lines 58-68 and column 11, lines 1-14, the column address decoder/selector units 1510-1530 are connected to the single data line pair and provide a pipeline stage.

Accordingly, it is clearly seen that the column address decoder/selector units do not, and can not, provide the width control signal, as in the presently claimed invention.

Thus, even combining the selected portion of *Takai* with *Smolansky, et al.*, that is, replacing the address decoder 102 of *Smolansky, et al.* with the column address decoder/selector units of *Takai*, it is respectfully submitted that the logic circuit as in the presently claimed invention would not have been rendered obvious.

Reconsideration is respectfully requested of claims 8, 9, and 17-19 under 35 U.S.C. 103(a), as being unpatentable over *Smolansky, et al.* and *Takai* in view of *Miyata, et al.*

These dependent claims recite the logic circuit construction that is part of the decoder and the switching circuit that is part of the data buffer controller.

Miyata, et al. relates to a control circuit for a memory.

Nevertheless, it is respectfully submitted that *Miyata, et al.* does not cure the deficiency of the primary references concerning the decoder construction and, thus, the claims 8 and 9,

which depend from claim 1, and claims 17-19, which depend from claim 10, are patentably distinct over the cited references.

Reconsideration is respectfully requested of the rejection of claims 22-24 under 35 U.S.C. 103(a), as being unpatentable over *Smolansky, et al.* and *Takai* and further in view of *Hirai*.

Claims 22-24 depend from independent claim 21 which, for the reasons set forth hereinabove, is thought to be patentably distinct over the cited references and, for at least those very same reasons, it is respectfully submitted that claims 22-24 are also submitted to be patentably distinct thereover.

Hirai relates to a communication apparatus, however, it is respectfully submitted that *Hirai* does not cure the deficiencies of the primary and secondary references as pointed out hereinabove.

Therefore, in view of the above remarks, it is respectfully submitted that a semiconductor memory device, as taught by the present invention and as recited in the amended claims, is neither shown nor suggested in the cited references, alone or in combination.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,
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